A Fault-Tolerant Series-Resonant DC-DC Converter

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Abstract—The Series-Resonant dc-dc converter (SRC) is widely used as power supply for telecommunications, wireless power transfer for electrical vehicle and high voltage power supplies. Recently it became very popular in Solid-State Transformer application, where fault tolerance is a highly desired feature and it is obtained through redundancy. This paper proposes a reconfiguration scheme for the SRC for the case of failure in one semiconductor, which could drastically reduce the need of redundancy. Using the proposed scheme, the full-bridge based SRC can be reconfigured in a half-bridge topology, in order to keep the converter operational even with the failure (open circuit or short circuit) of one switch. As a drawback of this technique, the output voltage drops to half of its original value. Therefore, a novel re-configurable rectifier based on the voltage doubler topology is proposed as a solution to keep the output voltage constant after the fault. To verify the feasibility of the proposed scheme, the converter is tested experimentally in a 700 V to 600 V prototype with 10 kW of output power. A IGBT short-circuit fault is tested and the results confirms the effectiveness of the proposed approach.

I. INTRODUCTION

The series-resonant dc-dc converter (SRC) has been very used in wireless power transfer application for electrical vehicle [1]–[4], battery charger [5], [6], renewable energy system [7]–[10] and high voltage power supply for specific application, such as traveling-wave tube (TWT) for satellite application [11]. Recently, this topology became very popular in Solid-State Transformer (SST) [12]–[14], mainly because of its characteristic of output voltage regulation in open loop. The SRC has been used for traction application [12], [13], where an efficiency of around 98% was achieved.

In SST, telecommunication or even in renewable energy system applications, the continuity of operation is of paramount importance. For that reason, a highly reliable system (preferable with redundancies) is required. The fault tolerant feature contributes to increase the availability of system and several fault tolerance methods have been proposed in literature [15]–[18]. Most of these methods includes a significant amount of extra hardware (such as semiconductors/leg redundancy [15], [17] or series connection of fuses/switches to isolate the fault [15], [16], [18]), increasing the cost and compromising the efficiency of the system. In this context, this paper proposes a fault tolerance solution with minimum of additional hardware and no impact on efficiency for the SRC converter, using the advantage of inherent fault tolerant capability of this topology.

Independently from the mechanism, there are two possible failures types for the semiconductor: open-circuit (OC) or short-circuit (SC). According to [19], [20], the reasons that implies a OC failure are: bond-wire lift off or rupture and failure on the gate drive. Meanwhile, the SC failure might be a result of an overvoltage, static or dynamic latch up, second breakdown or energy shock. Since most of the failures result

in a SC condition [19], this work focuses on a SRC resilient to SC failure.

The proposed reconfiguration scheme consists in re-configuring the full-bridge SRC (FB-SRC) in a half-bridge SRC (HB-SRC) converter. Nevertheless, the output voltage generated by the HB-SRC is half of the output generated by the FB-SRC, considering the same parameters. Therefore, a novel re-configurable rectifier based on the voltage-doubler topology is proposed in order to keep the same output voltage. The operation principle of the FB-SRC and HB-SRC operating in discontinuous conduction mode (dcm) are presented in Section II. In Section III, the reconfiguration scheme is described in detail and the proposed fault-tolerant topology is presented. Experimental results are provided in Section IV, in order to confirm the theoretical analysis developed in this paper. Finally, the conclusion is presented in Section V.

II. OPERATION PRINCIPLE OF THE SR CONVERTER

A. Full-Bridge SRC

The topology of the SRC based on full-bridge configuration (FB-SRC) is shown in Fig. 1 (a). To simplify the description, an unidirectional topology is considered in this analysis and a diode bridge rectifier is used in the secondary side. To support the analysis, the variables resonant frequency (f_o), resonant angular frequency (ω_0) and characteristic impedance of the resonant network (Z) are defined by (1), in terms of the resonant inductor (L_r) and capacitor (C_r) of the tank circuit.

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}, \quad \omega_0 = 2\pi f_0, \quad Z = \sqrt{\frac{L_r}{C_r}} \qquad (1)$$

Fig. 1 (c) shows the main waveforms for the FB-SRC operating at the resonant frequency ($f_s = f_o$) and below the resonant frequency ($f_s < f_o$), where f_s is the switching frequency. For operation below the resonant frequency, the current i_{Lr} reaches zero before half of the switching period, and it remains zero until the primary bridge applies negative output voltage, i.e. $v_p = -V_i$. Since the commutations happen when $i_{Lr} = 0$, all semiconductors switch at zero-current-switching (ZCS), avoiding therefore switching losses. Because of the soft-switching feature, this operation mode, named half-cycle discontinuous-conduction mode (dcm), is very advantageous and it will be considered for the analysis in this work. To operate at half-cycle dcm, the converter parameters must satisfy the following conditions [21]:

$$\gamma = \frac{\omega_0}{2f_s} > \pi \qquad (2)$$

$$f_s < f_0 \qquad (3)$$
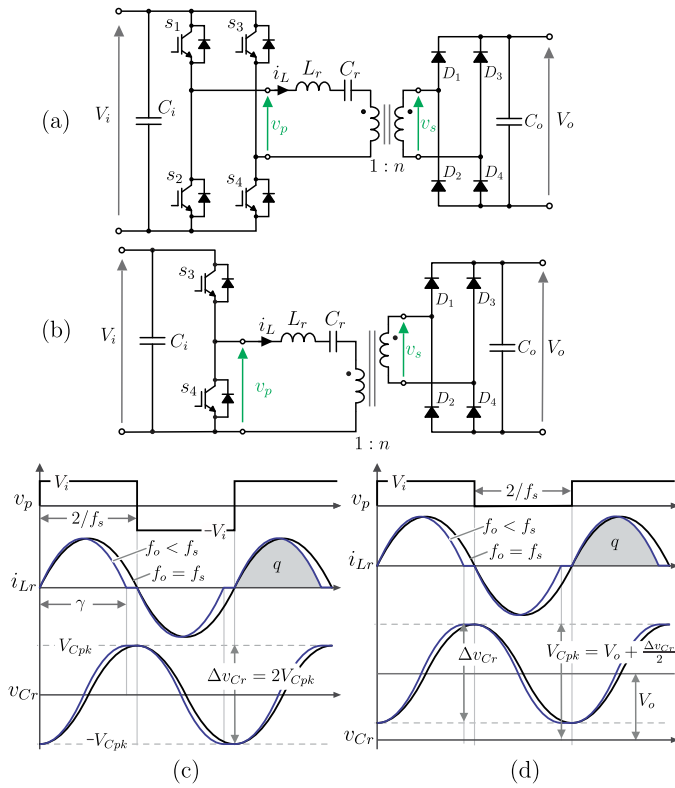
$$I_o < 8f_s C_r V_o \qquad (4)$$

Figure 1. Series Resonant dc-dc converter: (a) topology of the FB-SRC, (b) Topology of the HB-SRC, (c) main waveforms of the FB-SRC and (d) main waveforms of the HB-SRC.

where, γ is the angular length of one half switching period and I_o is the load current. From these conditions is possible to design L_r and C_r, considering the operation range of the converter.

The relation between the amount of charge stored in the capacitor (Δq) and its voltage (v_{Cr}) is given by (5). During the period $0 < t < T_0$ (where T_0 is the resonant period), the capacitor voltage starts from $-V_{Cpk}$ and reaches V_{Cpk} (see Fig. 1 (c)), thus $\Delta v_{Cr} = 2V_{Cpk}$. Likewise, the charge that flows through the capacitor during this period is defined as q, as shown in Fig. 1 (c). This relation is described in (6).

$$\Delta q = C_r \Delta v_{Cr} \tag{5}$$

$$q = 2 \cdot C_r \cdot V_{Cpk} \tag{6}$$

The instantaneous average value of the input current (i_i) is calculated by (7). As highlighted in this equation, the integral of the current during the time interval 0 to $T_s/2$ is the charge accumulated in the capacitor (see Fig. 1 (c)). Thus, the relation presented in (8) is found.

$$I_i = \langle i_1(t) \rangle_{Ts} = \frac{2}{T_s} \underbrace{\int_0^{T_s/2} i_1(t)dt}_{q} \tag{7}$$

$$I_i = 2f_s q \tag{8}$$

Replacing (8) in (6), (9) is obtained, and it can be rearranged to obtain the peak voltage on the capacitor in function of the

load (represented in this equation by the input current I_i), switching frequency and capacitance value, as presented in (10).

$$\frac{I_i}{2f_s q} = 2 \cdot C_r \cdot V_{Cpk} \tag{9}$$

$$V_{Cpk} = \frac{I_i}{8f_s C_r} \tag{10}$$

The output voltage of the converter is given by (11).

$$V_o = nV_i \tag{11}$$

B. Half-Bridge SRC

Besides the circuit shown in Fig. 1 (a), the series-resonant dc-dc converter can be also implemented based on the half-bridge topology (HB-SRC), as shown in Fig. 1 (b). This circuit became well-known in literature as LLC converter, due to the configuration of the tank circuit, considering the magnetizing inductance of the transformer, and it has been widely used in telecommunications power supply applications. The operation of the HB-SRC is very similar to the one of the FB-SRC converter, previously described. Therefore, equations (2) to (8) are still valid for the HB-SRC. The difference between these two converters lies on the resonant capacitor voltage (which has an offset of V_o in the HB-SRC converter, as shown in (12)) and also on the peak-to-peak value of the voltage v_p. As can be seen in Fig. 1 (c) and (d), the FB-SRC synthesizes an ac voltage v_p on the tank circuit input, with negative and positive values ($-V_i$, V_i), while the HB-SRC generates a rectangular waveform voltage v_p with zero and positive values (0, V_i). As a consequence, the output rectified voltage on the secondary side of the HB-SRC is given by (13), which is half of the value, when compared to the FB-SRC output voltage (see eq. (11)) for the same parameters (V_i and n). The main waveforms for the HB-SRC are shown in Fig. 1 (d).

$$V_{Cp} = \frac{I_i}{8f_s C_r} + V_o \tag{12}$$

$$V_o = \frac{nV_i}{2} \tag{13}$$

III. PROPOSED FAULT TOLERANT CONVERTER

As already mentioned, depending on the semiconductors failure mechanisms, the device will assume two possible states: open-circuit (OC) or short-circuit (SC) [19]. For voltage source converter, which is the case of the SRC, the OC fault is not catastrophic, since the power transfer will be naturally interrupted. Instead, the SC fault is the main issue, because it can cause destructive damage to the power converter. In addition, the SC failure type is mostly likely to happen in the real application than the OC failure. Therefore, the reconfiguration scheme proposed in this work is analyzed for the SC fault case, although it can also be used for the OC fault.
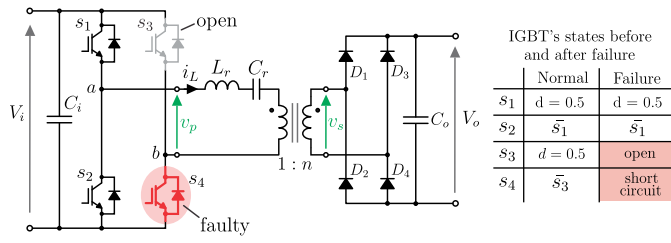
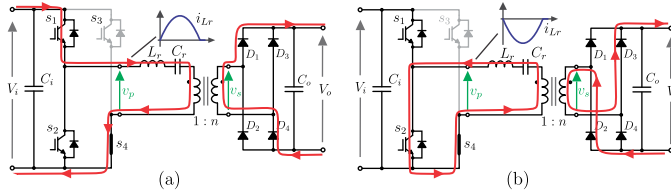Figure 2. FB-SRC under faulty condition: SC failure on the semiconductor s_4.

Figure 3. Operation of the FB-SRC as a HB-SRC after the reconfiguration. States operation of the SRC after the fault: (a) positive i_L current (first state), (b) negative i_L current (second state).

Figure 4. Main waveforms of the FB-SRC when a fault happens: main voltages and currents before and after the fault.

A. Reconfiguration Scheme: Operation and Control Level

The proposed reconfiguration scheme for the SRC consists in configuring the FB-SRC in a HB-SRC after the fault, i.e. SC of a semiconductor. The detailed analysis is carried out in this section for the FB-SRC shown in Fig. 2. Initially, as an example, it is assumed that the switch s_4 is damaged in SC (see Fig. 2), hence the switch s_3 must remain open, avoiding short-circuit of the input voltage source. Since the switch s_4 is short-circuited, the point b (highlighted in Fig. 2) is directly connected to the primary side ground and the damaged device is used as a circuit path, resulting in the same circuit of the Fig. 1 (b). Meanwhile, the healthy leg (composed of s_1 and s_2) operates normally. Fig. 3 shows the operation states of the SRC after the fault, i.e. after the reconfiguration, where it can be seen that the damaged switch s_4 being used as a circuit path. Fig. 4 shows the main waveforms of the FB-SRC when a fault happens.

As the HB-SRC provides only half of the output voltage compared to the FB-SRC, the output voltage of the converter after the fault will be half of its original value, which is not desired. Thereafter, to overcome this problem and keep the output voltage constant after the fault, a modification to the circuit of the secondary side rectifier is proposed and a novel re-configurable rectifier is obtained.

B. Fault-Tolerant SRC: Topology and Hardware Level

Fig. 5 (a) shows the topology of the standard full-bridge rectifier (FBR), which is the most used in the secondary side of the SRC [11], [3]- [10]. In this configuration, the output is given by: $v_o = v_{s_{pk}}$. Fig. 5(b) shows the topology of the voltage-doubler rectifier (VDR), which is also popular in the literature, however it has not so far been applied to the SRC. In this configuration, the rectified output voltage is given by: $v_o = 2v_{s_{pk}}$. Thus, in order to use the voltage doubler characteristic of the VDR in case of fault of the SRC, keeping its output voltage
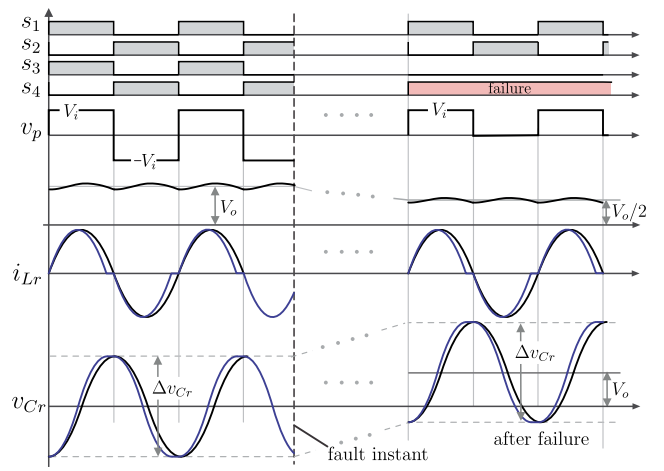
constant, a re-configurable rectifier circuit presented in Fig. 5 (c) is proposed. The proposed rectifier has two split capacitors and an additional switch (S_f) that allows to connect one side of the high frequency transformer secondary winding directly to the middle point of the capacitors, becoming a VDR.

The operation in normal and faulty conditions is depicted in Fig. 5 (d) and Fig. 5 (e), respectively. In normal operation, the switch S_f is open, and the rectifier operates as a standard FBR. In fault case, the switch S_f is on, and then the leg composed of the diodes D_3 and D_4 is bypassed. The bottom side of the secondary winding is connected to the middle point of the capacitors C_1 and C_2, as depicted in Fig. 2 (e). Therefore, the circuit operates as a VDR, and the output voltage value is twice the value in normal operation. Finally, Fig. 6 shows the complete proposed fault-tolerant series-resonant dc-dc converter (FT-SRC).

The main waveforms for the proposed FT-SRC before and after a failure are depicted in Fig. 7. As can be observed, before the failure (normal operation) the voltages v_p and v_{Cr} have an average value equal to zero and the output voltage is given by V_o. After the failure in the switch s_4 for example, there is the reconfiguration, in which the FB-SRC will operate as a HB-SRC and switch S_f is activated, so that the output stage can operate as the VDR. Consequently, the output voltage will remain in the same value, as desired. The effect of the reconfiguration is only observed on the voltage v_{Cr}, that has an expected offset of V_o, and on the the current i_{Lr}, that must be twice the previous value to process the same amount of power than before. Both characteristics are inherent of the HB-SRC.

To detect the fault and identify the faulty semiconductor, a fault detection and diagnosis method must be implemented. The main goal of this work is to propose the reconfiguration scheme for the SRC converter and to propose the FT-SRC, as already mentioned. Hence existing methods can be used to identify the failure in the proposed converter. It is well-know that the IGBT devices can withstand abnormal current during a short period of time, usually around 10 μs [20], [22], which is considerably large. Among the various methods that can be applied to this converter, *de-saturation detection method* [23],
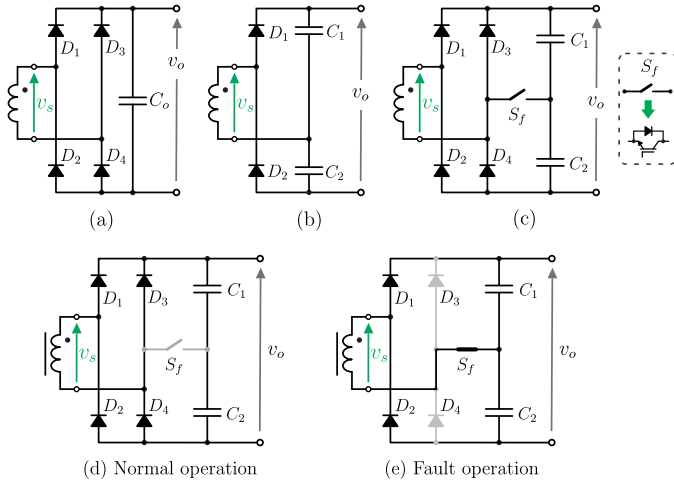
Figure 5. Possibles rectifier topologies and proposed topology: (a) full-bridge rectifier (FBR), (b) voltage-doubler rectifier (VDR) and (c) proposed reconfigurable rectifier. Operation of the proposed rectifier: (d) operation as a FBR, (e) operation as a VDR.
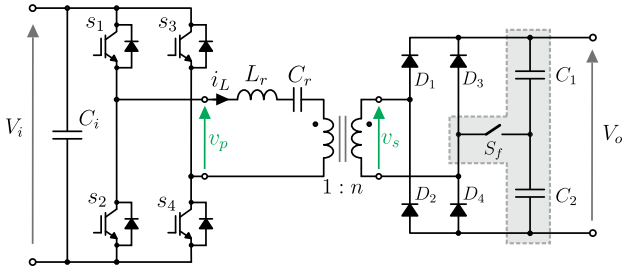

Figure 6. Proposed fault-tolerant SRC topology.

protection by gate voltage limiting, *current mirror method* [23] and *gate voltage sensing* [20] are very promised. All this indicated methods require the sensing of device collector voltage and/or current and therefore they are considerably simple to be implemented. Fig. 8 shows the protection method based on the *de-saturation detection* interfaced with the logic system, used to diagnosis the faulty leg. In case of fault of the switch s_4, the collector voltage of s_3 (v_{ceS3}) increases from the low saturation value to the dc link, while the gate signal is still high. In that case, the protection circuit disables the gate-drive (through the signal en_{HW}) and sends a signal ($FT3$) to the diagnosis system, to identify the faulty device. This method needs around $1\mu s$ to $5\mu s$ to detect the fault and actuate [20], protecting the device. Since the IGBT can withstanding a short-circuit current for $10\mu s$, the detection method is very suitable for this application.

In case of OC fault, the proposed solution is still valid. Instead of opening the healthy IGBT of the faulty leg, the logic system must close this IGBT. As an example, in case of OC fault of the switch s4, the switch s3 must remain closed, in order to be used as a path of the circuit. Therefore, to extend the proposed solution for OC fault actuation, only the logic system must be adjusted.

IV. EXPERIMENTAL RESULTS

In order to verify the performance of proposed FT-SRC converter and to attest the theoretical analysis presented in
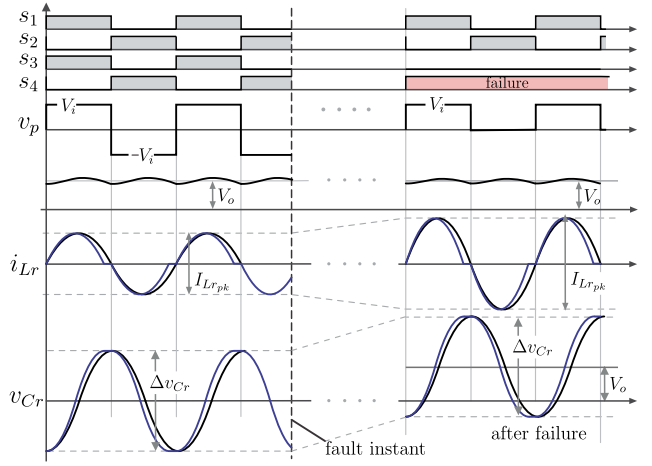

Figure 7. Main waveforms of the proposed FT-SRC when a fault happens: main voltages and currents before and after the fault.
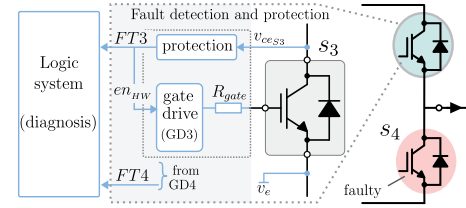

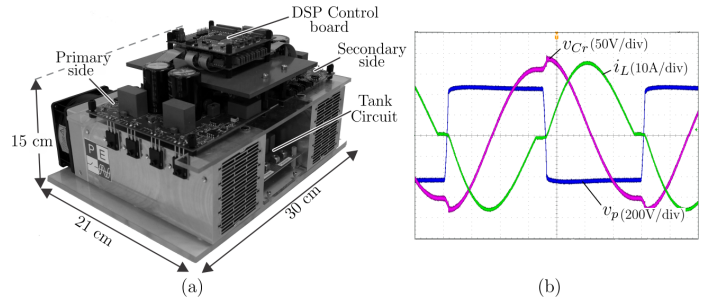Figure 8. Simplified gate-drive block diagram interfaced with the fault detection algorithm.

Figure 9. Implemented 10 kW fault tolerant SRC converter hardware prototype: (a) photo of the prototype (mechanical dimensions: 300 mm x 210 mm x 150 mm: power density: 1 kW/dm^3), (b) experimental result at nominal load ($V_i = 700$ V, $V_o = 600$ V, $P_o = 10$ kW), showing the operation of the prototype.

this paper, a 10 kW prototype was built and experimental results were obtained. The converter specifications are shown in Table I, while the resonant tank circuit parameters are shown in Table II. The prototype design was performed using the previous described equations. A 1.2 kV IGBT IHW40N120 was selected as the main switch and it was used on the primary side and secondary sides, in which the intrinsic diodes of the IGBT were used to rectifier. The converter operates in open loop and the gating signals are generated by the DSP. To evaluate dynamically the performance of the converter under fault case, a short-circuit on the switch s_2 was emulated by software in the DSP. No diagnosis method was used, since it is not the main focus of this paper.

Fig. 9 shows photo of the prototype and the main waveforms for the converter operating in steady-state at nominal condition. The results were obtained for the converter operating in

Table I
SPECIFICATION OF THE SRC PROTOTYPE

Input voltage	$V_i = 700$ V
Output voltage	$V_o = 600$ V
Nominal output power	$P_o = 10$ kW
Switching frequency	$f_s = 20$ kHz
Transformer turn ratio	$n = 1.45$

Table II
MAIN PARAMETERS OF THE TANK CIRCUIT

Resonant capacitance	$C_r = 0.68 \mu F$
Resonant Inductor	$L_r = 79 \mu H$
Tank resonant angular frequency	$\omega_0 = 1.364 \cdot 10^5$ rad/s
Resonant frequency	$f_o = 21.7$ kHz
Angular length of half switching period	$\gamma = 0.577$

steady-state (before and after the fault) and also dynamically during the fault and they are discussed herein. For safety reasons, the dynamic results were obtained for reduced input and output voltages.

Initially, the converter was tested considering only the reconfiguration scheme in the primary bridge, without the proposed re-configurable rectifier, in order to verify the inherent capability to withstand a fault of the SRC. The test was performed with input and output voltage of 200 V and 300 V, respectively, and the results for this condition are presented in Fig. 10. The dynamic response of the FB-SRC during the fault of the switch s_2 is depicted in Fig. 10 (a), in which is observed the the converter remains operational after the fault, proving its inherent ability to handle the fault, as described in Section III. As expected the output voltage drops to half of its value (from 300 V to 150 V) after the fault and the capacitor voltage has an offset of V_o. The inductor current is also reduced, because the test was performed with constant resistance as load and therefore reduction on the output voltage implies in reduction on power. The detailed waveforms before and after the fault can observed in the Figs. 10 (b) and (c), respectively.

Afterwards, the proposed FT-SRC (including the proposed rectifier) was tested, for an input voltage of 350 V and output voltage of 500 V and the main results are presented in Fig. 11. The dynamic behavior during the fault on switch s_2 of the proposed FT-SRC is shown in Fig. 11 (a) and as can be seen in this figure, the converter remains operational after the fault and it provides a constant output voltage (500 V) even after the fault, attesting the effectiveness of the proposed rectifier and the converter. As the output voltage remains constant, the amount of processed power is the same before and after the fault and therefore the amount of current on the resonant tank is twice after the fault, because of the HB configuration on the primary side. The detailed waveforms before and after the fault can observed in the Figs. 11 (b) and (c), respectively. To summarize, the results have shown that the proposed converter can handle a short-circuit fault in one device and still provide the required output voltage and power, keeping the continuity of operation.

V. CONCLUSION

This paper has proposed a fault-tolerant series-resonant dc-dc converter. The basic operation of the SRC based on the
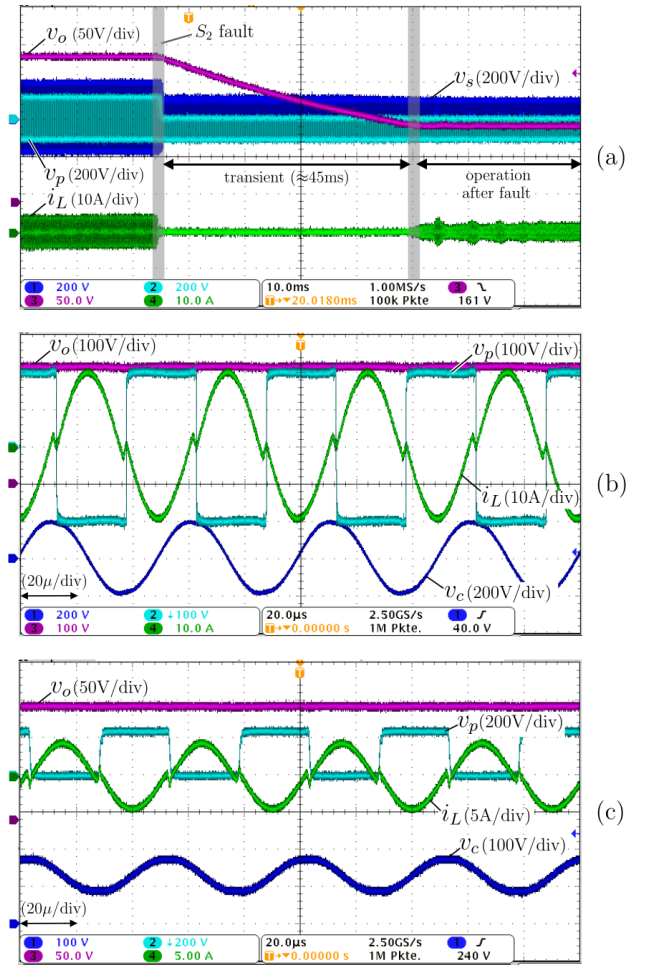

Figure 10. Experimental results of the FB-SRC (without the reconfigurable rectifier on the secondary side) under a fault on the switch s_2: (a) dynamic behavior of the converter during the fault, (b) steady-state operation before the fault and (c) steady-state operation after the fault.

full-bridge and half-bridge topologies was described. Then, a semiconductor short-circuit fault case is evaluated for the full-bridge series-resonant converter and a reconfiguration scheme, in which the FB-SRC operates as a HB-SRC, is presented. As a result of the reconfiguration, the output voltage is reduced. To overcome this problem a modified rectifier that can be reconfigured in a voltage doubler rectifier, keeping the output voltage constant, is proposed.

The main advantages of the proposed converter are: post-fault operation, simple implementation, reduced number of additional components and no efficiency deterioration. However, the resonant capacitor must be designed for higher voltage and the current effort on the healthy devices in failure mode operation is twice the than in normal mode operation.

Experimental results for a 10 kW prototype were obtained and the effectiveness and advantages of the proposed fault tolerant series resonant dc-dc converter has been demonstrated.

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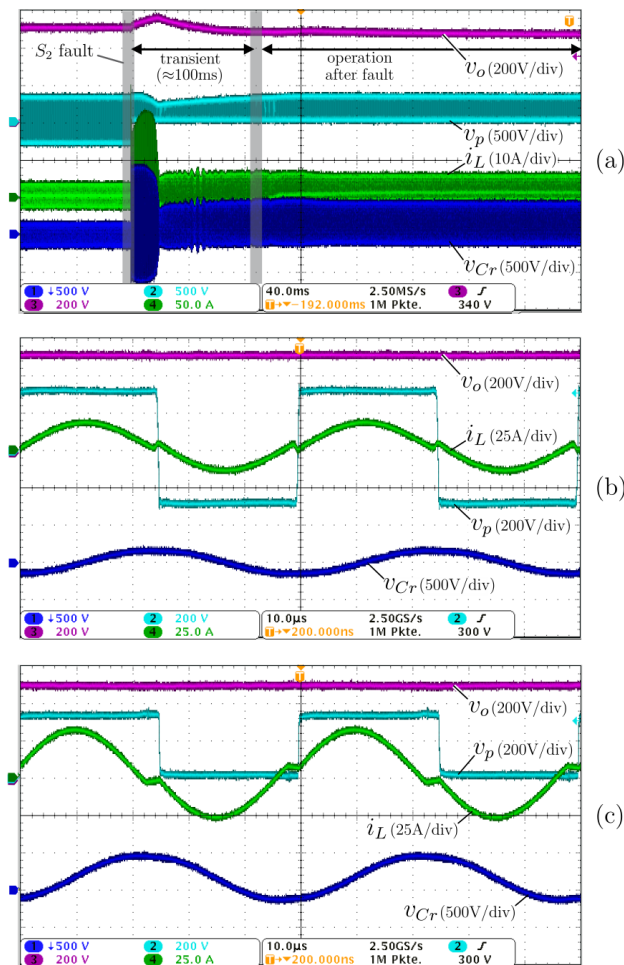
Figure 11. Experimental results of the proposed FT-SRC under a fault on the switch s_2: (a) dynamic behavior of the converter during the fault, (b) steady-state operation before the fault and (c) steady-state operation after the fault.

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